(19) JAPANESE PATENT OFFICE (JP)

(12) KOKAI TOKUHYO PATENT JOURNAL (A)

(11) PATENT APPLICATION PUBLICATION NO. 2002-281077

(43) Publication Date September 27, 2002

(51) Int. Cl.[7]:	Identification Codes:	FI		Theme codes (reference)
H04L 12/56	230	H04L	12/56	230A 5C059
7/00			7/00	Z 5K030
H04N 7/24		H04N	7/13	Z 5K047

Examination Request: Not filed

No. of Claims: 4 (Total of 10 pages)

(21) Filing No.: 2001-81074

(22) Filing Date: March 21, 2001

(71) Applicant: 000005108
Hitachi, Ltd.
4-6 Kandasurugadai,
Chiyoda-ku, Tokyo

(71) Applicant: 000003687
Tokyo Electric Power Company
1-1-3 Uchisaiwai,
Chiyoda-ku, Tokyo

(72) Inventor: Masaaki Takisawa
Network System Business
Department, Hitachi, Ltd.
6-27-6 Minami Oi,
Shinagawa-ku, Tokyo

(74) Agent: 100078134
Junjiro Takeshi, patent attorney

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(54) [Title] Signal reception device and signal reception method

(57) Abstract

Problem

To facilitate absorption of jitter of real-time transmission signals transmitted via IP or other packet network having a lot of jitter and to restrain the time delay needed for absorbing the jitter.

Means to solve

The device of the present invention has a means 11 that stores time stamp CR for RTP and MPEG-2 system layers in the same de-jitter buffer 13, a means 15 that calculates time TCd corresponding to the storage amount 19 of de-jitter buffer 13, and a means 18 that compares CR to time TCd on the reading side of the de-jitter buffer and control reading when they are consistent with each other.

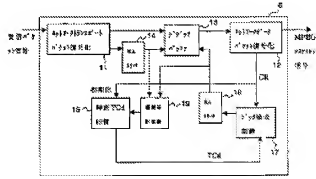

Figure 2 translated at end of document

There are no amendments to this patent.

Claims

1. A signal reception device that receives real-time signals via a packet network, characterized by having a means that stores the time stamp signal used for transmitting the time information on the transmission side and the real-time signal in the same buffer memory, a means that recovers the clock on the transmission side and the time information corresponding to the storage amount of the buffer memory, and a means that compares said time stamp to the recovered time information on the reading side of the buffer memory and reads out the real-time signal from the buffer memory when they are consistent with each other.

2. The signal reception device cited in Claim 1, characterized by the fact that the means that recovers the clock on the transmission side and the time information has a means that derives the difference between the storage amount of said buffer memory and a predetermined threshold value, a means that multiplies weight 1 by said difference if the storage amount of the buffer memory is equal to or larger than the predetermined threshold value and multiplies a large weight depending on said difference if the storage amount of the buffer memory is smaller than the predetermined threshold value, and a means that recovers said clock by using a value obtained by smoothing the result of multiplying the weight by the difference in the time direction.

3. A signal reception method that receives real-time signals via a packet network, characterized by the following facts: the time stamp signal used for transmitting the time information on the transmission side and the real-time signal are stored in the same buffer memory; the clock on the transmission side and the time information corresponding to the storage amount of the buffer memory are recovered; said time stamp is compared to the recovered time information on the reading side of the buffer memory, and the real-time signal is read out from the buffer memory when they are consistent with each other.

4. The signal reception method cited in Claim 3, characterized by the following facts: the difference between the storage amount of said buffer memory and a predetermined threshold value is derived; weight 1 is multiplied by said difference if the storage amount of the buffer memory is equal to or larger than the predetermined threshold, and a large weight depending on said difference is multiplied if the storage amount of the buffer memory is smaller than the predetermined threshold value; said clock is recovered by using a value obtained by smoothing the result of multiplying the weight by the difference in the time direction.

Detailed explanation of the invention

[0001]

Technical field of the invention

The present invention relates to a signal reception device and a signal reception method. In particular, the present invention relates to a signal reception device and a signal reception method that can receive real-time encoded video or audio signals, which are transmitted at a constant rate, on the reception side appropriately to restrain jitter and minimize the time delay when the signals are transmitted via an IP or other packet network, which is commonly used but has a great deal of so-called jitter that causes early or late arrival of the signals.

[0002]

Prior art

Various kinds of conventional technologies have been developed for image encoding systems. Examples include the fixed-length coding method that assigns a certain codeword length for each sample point (pixel) of the image signal and the variable-length coding method that assigns codewords with variable length. The variable-length coding method has a complicated configuration. However, since a codeword with the optimal length can be assigned corresponding to the incident occurrence probability, the average codeword length can be substantially shortened, and the transmission efficiency can be improved. Therefore, the variable-length coding method is widely adopted.

[0003]

For variable-length coding, however, since the codeword length is different for each screen, it is necessary to synchronize the screens on the transmission side and the reception side. Therefore, on the transmission side, the value of the time information known as STC is obtained at a period of, for example, 100 ms and is transmitted to the reception side as time information (time stamp) known as PCR. On the reception side, the transmitted time stamp PCR is used to recover time STC to decode the video and audio signals. To recover time STC, a system clock with a predetermined frequency is used and counted by a counter on the reception side to form time STC, and the time STC is compared to the received time stamp PCR. The frequency of the aforementioned system clock is increased or decreased to keep the compared times consistent.

[0004]

Since the aforementioned system clock is used in the entire decoding device, image display is also regulated by that system clock. Therefore, when the system clock significantly deviates from the normal frequency, the image monitor cannot display the picture. Also, when

the system clock varies in a relatively short period, even if the deviation is small, the clock generated by the voltage controlled oscillator for demodulating color difference signal of the image monitor varies corresponding to that variation and cannot be cut off. As a result, color unevenness or other problems may occur.

[0005]

When an ATM network or special line network with less jitter is used as the transmission path, since time stamp PCR also arrives with less jitter, the system clock and time STC can be easily recovered on the reception side. However, as can be seen from the aforementioned system clock generating method, if there is a lot of so-called jitter with the reception time of time stamp PCR transmitted at a certain period varying significantly without following the aforementioned period on the reception side, it is unable to correctly compare the aforementioned PCR to the time STC when the PCR arrives, making it difficult to correctly recover the system clock or time STC. In other words, as described above, it is unable to display picture on the image monitor, and color unevenness or other problems may occur.

[0006]

Jitter occurs in a packet network for the following reason. Since a packet network is formed in order to transmit non-real time data in a reliable manner, it is constituted appropriately to transmit data that only burst for a certain period of time. In other words, a device known as a router or the like is used for the network nodes that constitute the packet network. After temporarily storing the received signals in a memory, the aforementioned router will transmit the signals only when there is margin for transmission to a network. Therefore, different data are stored for different periods in the router. Also, if the amount of data in the actual stream increases compared to the transmission capacity, the waiting time in the router will increase. Therefore, the overall delay will be increased, and the jitter is also increased.

[0007]

The technology disclosed in "Example 1 of H.222.0 Annex J.2 of ITU advice" is an example of the prior art (first prior art) for solving the aforementioned problem. According to the aforementioned first prior art, before the aforementioned time stamp PCR is received on the reception side, the data are temporarily stored in a FIFO (buffer memory known as “first in, first out”), and the data are read out from the FIFO at a constant rate so that the storage amount of the FIFO is stabilized at a certain amount (for example, half-full). According to this method, when the variation in the arrival rate of the received signal, that is, the jitter is large, the storage amount of the FIFO also varies. Therefore, the rate of reading data from the FIFO must be

changed corresponding to the variation in the storage amount. Consequently, this method can be applied to an ATM network or the like when there is a relatively small amount of jitter. When the jitter of the input signals is extremely large like in packet network, it is difficult to apply the aforementioned method because the reading rate from the FIFO will also vary corresponding to the jitter.

[0008]

In general, an MPEG-2 decoding device performs decoding at a regulated reading rate and also displays image on an image monitor based on the aforementioned rate. It is a well-known fact that the secondary carrier frequency used for transmitting the color difference signal of image signals to display on an image monitor is about 200-3000 ppm. If the frequency deviates from the regulated frequency: 3.579 MHz, the colors cannot be reproduced. Consequently, if the reading rate has serious jitter, jitter also occurs in the image signals output to the image monitor using the aforementioned reading rate, and the secondary carrier frequency departs from the regulated value to exceed the pull-in range of the image monitor. As a result, it may be unable to reproduce the color signals.

[0009]

Another technology disclosed in "Example 2 of H.222.0 Annex J.2 of ITU advice" (second prior art) is used to solve the aforementioned problem. The second prior art is realized by carrying out the following procedure.

[0010]

(1) In a network adaptation layer (the method known as RTP: real time protocol is used for an IP network), the time for RTP known as TC is extracted from the time stamp known as CR provided in the RTP layer by means of PLL (phased lock loop) or other technology.

[0011]

(2) Time TCd is calculated by subtracting the time needed for absorbing the jitter (J/2: J represents the peak-to-peak value of the jitter) from said time TC.

[0012]

(3) The data received via a packet network are separated into MPEG-2 system layer and said CR, which are stored in a de-jitter buffer and a jitter removal control circuit, respectively.

[0013]

(4) The jitter removal control circuit compares the time TCd generated in said (2) to the stored CR and reads out the signals of the MPEG-2 layer corresponding to that CR when they are consistent with each other.

[0014]

(5) An MPEG-2 decoding device generates the system clock for decoding of time STC from the time stamp PCR within the MPEG-2 system layer and carries out normal decoding.

[0015]

(6) In this way, a normal reception device that can absorb large jitter generated by a packet network can be constituted.

[0016]

Figure 5 is a block diagram illustrating the configuration of an IP signal reception device based on the aforementioned second prior art. Figure 6 is a block diagram illustrating the configuration of the time recovery circuit in Figure 5. In the following, the prior art will be explained based on these figures. In Figures 5 and 6, 6 represents an IP signal reception device. 11 represents a network transport packet decoding circuit. 12 represents a network data packet decoding circuit. 13 represents a de-jitter buffer. 14 represents a write address (WA) counter. 15 represents a time (TC) recovery circuit. 16 represents a differential circuit. 17 represents a jitter removal control circuit. 18 represents a read address (RA) counter. 31 represents a counter. 32 represents a comparison circuit. 33 represents a smoothing circuit. 34 represents a voltage controlled oscillator.

[0017]

In signal reception device 6 shown in Figure 5, for the received packet signals, only the signals to receive are received by network transport packet decoding circuit 11, and the headers or the like of the packets of the transport layer are removed. The network data are transferred to network data packet decoding circuit 12. Network data packet decoding circuit 12 decomposes the packets and extracts time stamp CR for RTP. Time stamp CR is written into time recovery circuit 15 and jitter removal control circuit 17, and the MPEG-2 system layer signal is written into de-jitter buffer 13. The write address of de-jitter buffer 13 is regulated by WA counter 14.

[0018]

Time recovery circuit 15 recovers time TC from time stamp CR. In order to restrain underflow of de-jitter buffer 13 caused by the jitter, differential circuit 16 subtracts value J/2 obtained by multiplying the peak-to-peak value of the jitter from TC by 1/2 to generate delay time TCd. Time TCd is notified to jitter removal control circuit 17.

[0019]

Jitter removal control circuit 17 stores time stamp CR and delays it in synchronization with the corresponding MPEG-2 system layer signal stored in de-jitter buffer 13 and compares it to time TCd. If they are the same, read address counter 18 is incremented, and the corresponding MPEG-2 system layer signal is read out from de-jitter buffer 13.

[0020]

Since the value of TC is synchronized with time TC on the transmission side, the signal reception device 6 shown in Figure 5 that operates as described above can read out the MPEG-2 system layer signal from de-jitter buffer 13 after a certain time delay (J/2), since the time when time stamp CR is provided on the transmission side and can theoretically remove the jitter. Also, even if there is some jitter in the system clock recovered on the reception side, the image monitor that does not graphically display the MPEG-2 system layer signal can display the picture without problem as long as the color difference signal is within the allowed pull-in range.

[0021]

Time recovery circuit 15 in said signal reception device 6 is constituted as shown in Figure 6. Then, counter 31 is initialized to the value of CR provided from network data packet decoding circuit 12. After that, every time CR is provided, the value of the provided CR is compared to the value of counter 31 by comparison circuit 32. After the comparison result is smoothed by smoothing circuit 33, it is input into voltage controlled oscillator 34, and the clock is recovered. The clock is input into counter 31 to increment the value of the counter. This clock is almost synchronized with the clock that generates CR on the transmission side. The value of counter 31 is also almost consistent with the value of the counter that generates CR on the transmission side. They are not exactly the same because the time difference between the transmission time on the transmission side and the arrival time on the reception side is not constant due to the jitter of CR. Time recovery circuit 15 can almost correctly reproduce the clock or time of the transmission side on the reception side as described above.

[0022]

The aforementioned second prior art reproduces not only the direct reading clock from the remaining amount of the FIFO but also the clock known as TC from the received CR. TC is 90 kHz irrespective of the transmission rate or the jitter. The clock on the transmission side that generates CR is also 90 kHz, and its value is generated from a camera signal. Therefore, the frequency accuracy of the camera signal can be guaranteed. It is known that the accuracy of normal camera signals is as high as ±10 ppm. Therefore, if the pull-in range of the clock on the reception side is set to about ±100 ppm, the clock on the reception side can have a sufficient margin and can be synchronized with the clock on the transmission side. It can also be restrained within the pull-in range of the image monitor.

[0023]

Problems to be solved by the invention

The aforementioned second prior art can better restrain jitter than the first prior art. However, since the time stamp CR for RTP and the signal of the MPEG-2 system layer are stored separately, management becomes complicated, and it is difficult to miniaturize the device or realize good cost effectiveness. Also, since CR is transmitted at equal intervals on the transmission side in the second prior art, when it is used for an ATM network or the like having less jitter, the CR also arrives at almost equal intervals, and it is relatively easy to reproduce TC from this CR. However, when it is used for a packet network or other network having large jitter, since CR does not arrive at equal intervals, complicated logic computation is needed in order to reproduce TC from CR. As a result, the circuit scale is increased.

[0024]

In the aforementioned second prior art, the value used for jitter absorption is calculated by subtracting J/2 from TC, and the MPEG-2 system layer corresponding to each CR is read out. When J/2 varies dynamically, it is impossible to absorb or cut off the jitter. As a result, the de-jitter buffer underflows, and a transmission error occurs. Or, when the de-jitter buffer has excessively high absorbability, the MPEG-2 system layer signal may be significantly delayed. Therefore, the objective of the present invention is to provide a signal reception device and a signal reception method that can facilitate absorption of jitter of real-time transmission signals transmitted via an IP or other packet network having a lot of jitter and to restrain the time delay needed for absorbing the jitter.

[0025]

Means to solve the problems

In order to realize the aforementioned objective, the present invention provides a signal reception device that receives real-time signals via a packet network. This signal reception device has a means that stores the time stamp signal used for transmitting the time information on the transmission side and the real-time signal in the same buffer memory, a means that recovers the clock on the transmission side and the time information corresponding to the storage amount of the buffer memory, and a means that compares said time stamp to the recovered time information on the reading side of the buffer memory and reads out the real-time signal from the buffer memory when they are consistent with each other.

[0026]

That is, more specifically, the device of the present invention has a means that stores time stamp CR for RTP and the MPEG-2 system layer in the same de-jitter buffer, a means that calculates time TCd corresponding to the storage amount of the de-jitter buffer, and a means that compares CR to time TCd on the reading side of the de-jitter buffer and reads out from the de-jitter buffer when they are consistent with each other.

[0027]

Embodiment of the invention

In the following, the embodiment of the signal reception device disclosed in the present invention will be explained in detail with reference to figures.

[0028]

Figure 1 is a block diagram illustrating the overall configuration of a system that transmits video signals, audio signals, and other real-time signals by using a packet network. First, the configuration of the system that transmits video signals, audio signals, and other real-time signals by using a packet network, to which the present invention is applied, will be explained with reference to Figure 1. In Figure 1, 1 represents a camera, 2 represents a microphone, 3 represents an image/sound encoding device, 4 represents a packet signal transmission device, 5 represents a packet network, 6 represents a signal reception device, 7 represents an image/sound decoding device, 8 represents an image monitor, and 9 represents a speaker.

[0029]

In the system shown in Figure 1, the video signals picked up by camera 1 and the audio signals collected by microphone 2 are encoded by image/sound encoding device 3. After being converted to a form suitable for the IP network by the packet signal transmission device, these signals are output to packet network 5. After receiving the packet signals transmitted from IP transmission network 5 and inversely converting them to an appropriate form, packet signal reception device 6 transfers these signals to image/sound decoding device 7. Image/sound decoding device 7 recovers the video signals and the audio signals in a procedure opposite the encoding procedure in image/sound encoding device 3 and outputs the signals to image monitor 8 and speaker 9.

[0030]

Figure 2 is a block diagram illustrating the configuration of the signal reception device disclosed in an embodiment of the present invention. Figure 3 is a diagram explaining variation in the data storage amount in the de-jitter buffer. Figure 4 is a block diagram illustrating the configuration of the time recovery circuit in Figure 2. In Figures 2 and 4, 19 represents a storage amount counter, 21 represents a differential circuit, 22 represents a positive/negative judgment circuit, 23 represents a switch, 24 represents a multiplier circuit, 25 represents an averaging circuit, 26 represents a voltage controlled oscillator, and 27 represents a counter. The symbols of the terminals are the same as those shown in Figure 5.

[0031]

In signal reception device 6 disclosed in the embodiment of the present invention shown in Figure 2, for the received IP signal, the packet header of the transport layer is removed by network transport packet decoding circuit 11 in the same way as in the prior art explained based on Figure 5 to generate network data packet. The network data packet is directly written into de-jitter buffer 13. The write address is regulated by WA counter 14.

[0032]

The storage amount of de-jitter buffer 13 obtained by counting the difference between WA counter 14 and RA counter 18 with storage amount counter 19 is input into time recovery circuit 15. Then, time recovery circuit 15 controls the rate of the system clock such that the value obtained by averaging the storage amount of 13 over time is constant and generates time TCd on the reception side from the system clock. That is, time recovery circuit 15 speeds up the system clock in order to increase the reading rate when the average value of the stage amount of de-jitter

buffer 13 is increased and delays the system clock to delay TCd when the average value of the storage amount is reduced.

[0033]

The fact that time recovery circuit 15 disclosed in the aforementioned embodiment of the present invention generates system clock from the storage amount is the same as that in the first prior art explained above. In the embodiment of the present invention, however, the frequency of the system clock is synchronized with the system clock on the transmission side. That is, since it is known that the system clock frequency on the transmission side is stable to about ±10 ppm, the control range of the system clock frequency on the reception side can be limited to about ±100 ppm as in the second prior art explained based on Figure 5. Consequently, the jitter of the image signals generated from such a system clock can be restrained to ±200-300 ppm or lower so that the color difference signals can be reproduced so that normal display can be performed.

[0034]

Time recovery circuit 15 is initialized as follows. That is, at the time of initializing time recovery circuit 15, de-jitter buffer 13 performs idle reading until time stamp CR is detected. When CR is detected, the reading operation is stopped. Then, when the storage amount of de-jitter buffer 13 reaches a predetermined value, reading of de-jitter buffer 13 is started, and the value of CR is written into time recovery circuit 15 to initialize time recovery circuit 15.

[0035]

Network data packet decoding circuit 12 extracts CR from the network data packet read out from de-jitter buffer 13 by RA counter 18 and notifies it to jitter removal control circuit 17. It also eliminates the header of the network data packet and transfers the MPEG-2 system layer signal to image/sound decoding device 7 shown in Figure 1.

[0036]

Jitter removal control circuit 17 compares TCd to CR and, if they are consistent with each other, increments RA counter 18 and reads out from de-jitter buffer 13.

[0037]

The signal reception device disclosed in the embodiment of the present invention has the aforementioned configuration and carries out the processing operation as described above. In this way, the same operation as that of the second prior art can be realized by a simpler circuit.

[0038]

The aforementioned embodiment of the present invention can reduce the time delay while absorbing jitter by using the method to be explained below since it is characterized by using the storage amount to generate TCd.

[0039]

That is, as the evaluation function during recovery of time TCd, when the storage amount is equal to or larger than the threshold value, the absolute value of the difference between the storage amount and the threshold value is added. When the storage amount is smaller than the threshold value, the absolute value of the aforementioned difference is subtracted for smoothing. In this case, as shown in Figure 3(a), the average time delay becomes constant whether the jitter is large or small. On the other hand, in order to reduce the storage amount as much as possible, as shown in Figure 3(b), a relatively small threshold value is set. When the storage amount is equal to or larger than that threshold value, the absolute value of the difference between the storage amount and the threshold value is added. When the storage amount is smaller than the threshold value, a large weight N is multiplied by the absolute value of the difference between the threshold value and the storage amount, followed by subtraction to be averaged. Since the ratio of the area of the region in which the time delay is larger than the threshold value to the area of the region in which the time delay is smaller than the threshold value becomes the reciprocal of said weight, the area of the region in which the time delay is smaller than the threshold value decreases as weight N (N, for example, can have a value of about 10-100) increases. Consequently, variation in the storage amount in the case when weight is applied becomes that shown in Figure 3(b). When the jitter magnitude decreases, the storage amount is reduced, and the time delay can be reduced. Also, when the jitter increases, the minimal value of the storage amount barely changes. However, the average value is increased. In this way, the time delay can be increased automatically so that underflow in de-jitter buffer 13 can be prevented.

[0040]

The aforementioned threshold value can also be set to the minimal value at which underflow occurs in de-jitter buffer 13 within the assumed range of the jitter.

[0041]

In the following, an example of time recovery circuit 15 having an averaging circuit that changes the weight depending on whether the difference between the aforementioned threshold value and the storage amount is positive or negative will be explained with reference to Figure 4.

[0042]

The storage amount of de-jitter buffer 13 as the difference between WA counter 14 and RA counter 18 is calculated by storage amount counter 19, and the result is input into time recovery circuit 15. As shown in Figure 4, time recovery circuit 15 comprises differential circuit 21, positive/negative judgment circuit 22, weight selecting switch 23, multiplier circuit 24, averaging circuit 25, voltage controlled oscillator 26, and counter 27.

[0043]

In time recovery circuit 15 shown in Figure 4, differential circuit 21 calculates the difference between the storage amount of de-jitter buffer 13 and the threshold value. It is determined by positive/negative judgment circuit 22 whether the calculated difference is positive or negative. "1" or a larger value "N" is selected by switch 23 as the weight depending on the judgment result. Multiplier circuit 24 multiplies the selected weight by the output of differential circuit 21. The result is smoothed by averaging circuit 25 and is input into the control terminal of voltage controlled oscillator 26. Voltage controlled oscillator 26 increases/decreases the frequency of the system clock corresponding to the voltage of the control terminal. The system clock is provided to counter 27. Counter 27 generates time TCd. Consequently, said time TCd is controlled appropriately to lead or lag in accordance with the storage amount of de-jitter buffer 13.

[0044]

If the value of the aforementioned weight is "1," it is simply averaged as shown in Figure 3(a).

[0045]

In the embodiment of the present invention explained above, the time stamp CR used for transmitting the time information on the transmission side and the real-time signal obtained by encoding the image or the like are stored in the same buffer memory. The clock and time information on the transmission side are recovered corresponding to the storage amount of the buffer memory. The aforementioned time stamp CR is compared to the recovered time information on the reading side of the buffer memory. If they are the same, the real-time signal is read out. The present invention, however, can be modified as follows.

[0046]

That is, the present invention can also assign numbers sequentially to packets as a measure against packet loss. For example, MPEG over IP has a protocol known as Real Time Protocol (referred to as RTP hereinafter). A sequence number is assigned to each packet. The method realized by adopting the aforementioned protocol can detect packet loss or abandonment because the received sequence numbers become discontinuous if a packet does not arrive or an arrived packet is discarded because of parity error or the like.

[0047]

If the aforementioned protocol is adopted in the aforementioned embodiment of the present invention, when packet loss or abandonment occurs, the storage amount of de-jitter buffer 13 is reduced, and the control with respect to time recovery circuit 15 is carried out unnecessarily in the direction of delaying the system clock frequency. In order to prevent this, according to the present invention, when packet loss or packet abandonment is detected as described above, a pseudo signal corresponding to the loss of a discarded packet is written into de-jitter buffer 13 at the address corresponding to the packet number. When the pseudo signal is read out from de-jitter buffer 13, it is erased, thereby eliminating the influence on the storage amount.

[0048]

Also, in the aforementioned embodiment of the present invention, MPEG-2 system signals are received. The present invention can also be used for receiving signals in systems that transmit any real-time signal having a time stamp.

[0049]

According to the aforementioned embodiment of the present invention, since the MPEG-2 system data or other real-time signals and the time stamp CR are stored in the same buffer memory, it is easy to correlate these signals to facilitate control of the signal reception. Also, according to the embodiment of the present invention, since the storage amount of the buffer memory is used to recover the time on the reception side, it is possible to minimize the storage amount of the signals in the buffer memory within the range that can absorb the jitter so that the time delay caused by buffering can be restrained to the minimum as demanded.

[0050]

Effect of the invention

As explained above, according to the present invention, the jitter that occurs when transmitting real-time signals by a packet network can be restrained on the reception side, and the time delay can be minimized.

Brief description of figures

Figure 1 is a block diagram illustrating the overall configuration of a system that transmits video signals, audio signals, and other real-time signals by using a packet network.

Figure 2 is a block diagram illustrating the configuration of the signal reception device disclosed in an embodiment of the present invention.

Figure 3 is a diagram explaining variation in the data storage amount in the de-jitter buffer.

Figure 4 is a block diagram illustrating the configuration of the time recovery circuit shown in Figure 2.

Figure 5 is a block diagram illustrating an example of the configuration of the signal reception device based on a prior art.

Figure 6 is a block diagram illustrating the configuration of the time recovery circuit shown in Figure 5.

Explanation of symbols

1 Camera
2 Microphone
3 Image/sound encoding device
4 Packet signal transmission device
5 Packet network
6 Signal reception device
7 Image/sound decoding device
8 Image monitor
9 Speaker
11 Network transport packet decoding circuit
12 Network data packet decoding circuit
13 De-jitter buffer
14 Write address (WA) counter
15 Time (TC) recovery circuit
16, 21 Differential circuit

17 Jitter removal control circuit
18 Read address (RA) counter
19 Storage amount counter
22 Positive/negative judgment circuit
23 Switch
24 Multiplier circuit
25 Averaging circuit
26 Voltage controlled oscillator
27 Counter
31 Counter
32 Comparison circuit
33 Smoothing circuit
34 Voltage controlled oscillator

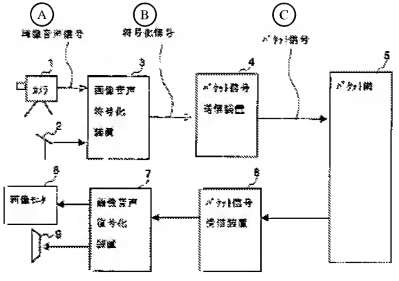

Figure 1

Key
A Video and audio signals
B Encoded signals
C Packet signals
1 Camera
3 Image/sound encoding device
4 Packet signal transmission device
5 Packet network
6 Signal reception device
7 Image/sound decoding device
8 Image monitor

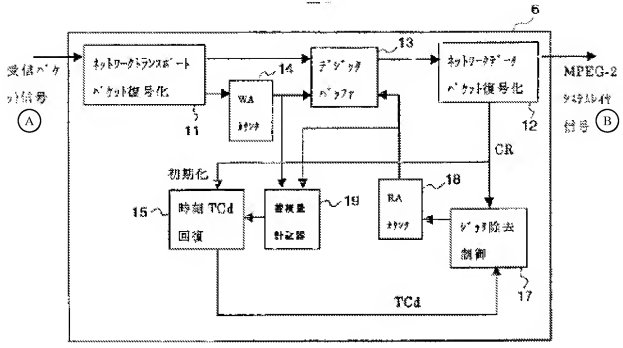

Figure 2

Key
- A Received packet signal
- B MPEG-2 system layer signal
- 11 Network transport packet decoding circuit
- 12 Network data packet decoding circuit
- 13 De-jitter buffer
- 14 WA counter
- 15 Time (TCd) recovery circuit
- 17 Jitter removal control circuit
- 18 RA counter
- 19 Storage amount counter

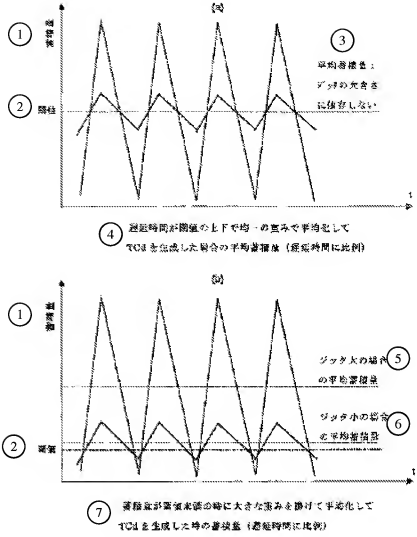

Figure 3

Key
1 Storage amount
2 Threshold value
3 Average storage amount: Irrespective of the magnitude of the jitter
4 Average storage amount (in proportion to the time delay) in the case when the time delay [sic; possibly storage amount] is averaged by using a uniform weight whether it is larger or smaller than the threshold value to generate TCd
5 Average storage amount when jitter is large
6 Average storage amount when jitter is small
7 Storage amount (in proportion to time delay) when the storage amount is averaged by being multiplied by a large weight when it is smaller than the threshold value to generate TCd

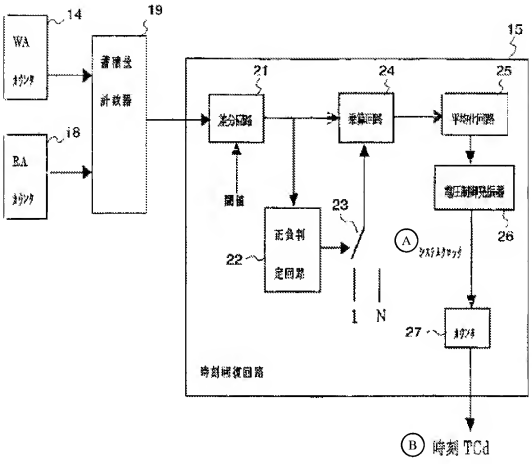

Figure 4

Key

	A	System clock
	B	Time TCd
	14	WA counter
	15	Time recovery circuit
	18	RA counter
	19	Storage amount counter
	21	Differential circuit
	22	Positive/negative judgment circuit
	24	Multiplier circuit
	25	Averaging circuit
	26	Voltage controlled oscillator
	27	Counter

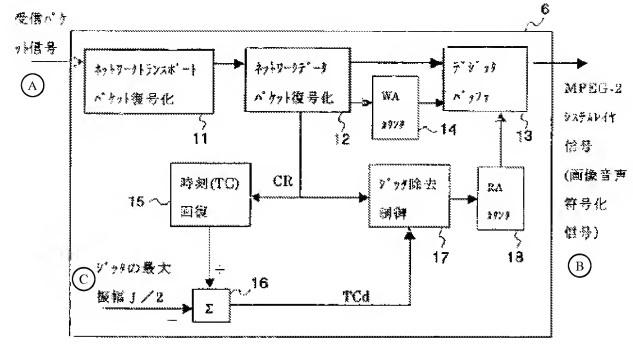

Figure 5

Key
A Received packet signal
B MPEG-2 system layer signals (encoded video and audio signals)
C Maximum amplitude of jitter J/2
11 Network transport packet decoding circuit
12 Network data packet decoding circuit
13 De-jitter buffer
14 WA counter
15 Time (TC) recovery circuit
17 Jitter removal control circuit
18 RA counter

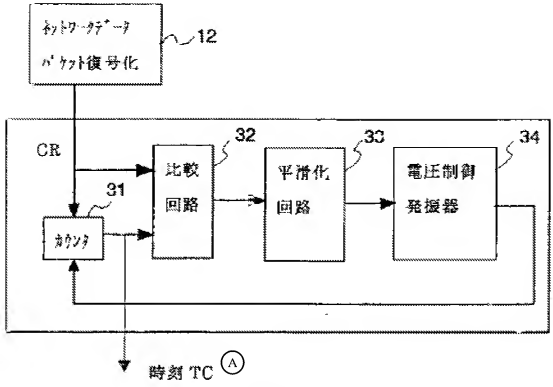

Figure 6

Key
A Time TC
12 Network data packet decoding circuit
31 Counter
32 Comparison circuit
33 Smoothing circuit
34 Voltage controlled oscillator

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(72) Inventor: Nobuyoshi Torii
Network System Business Department,
Hitachi, Ltd.
216 Totsuka-cho, Totsuka-ku,
Yokohama-shi, Kanagawa-ken

(72) Inventor: Shin Takare
Network System Business Department,
Hitachi, Ltd.
216 Totsuka-cho, Totsuka-ku,
Yokohama-shi, Kanagawa-ken

(72) Inventor: Yuji Omori
System Research Lab,
Tokyo Electric Power Company
4-1 Egasaki-cho, Tsurumi-cho,
Yokohama-shi, Kanagawa-ken

F Terms (reference)

5C059 KK00 MA00 RR02 RC04 RC32
SS30 TA71 TB04 TC15 TC45
TD11 UA32 UA38
5K030 GA11 HA10 HB02 HB15 HB28
KA03 KA21 MB15
5k047 AA06 AA18 BB15 DD02 GG09
MM12 MM24